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Study of Various Design & Performance Aspects of Mosfets at Nanometer Technology

Ankita Wagdre*, Shashank Mane**
*(Research Scholar, Department of Electronics & Communication, SBITM, Betul, 460001)
** (Department of Electronics & Communication, SBITM, Betul, 460001)

ABSTRACT
As per the International Technology Roadmap for Semiconductors (ITRS) each lower node is 0.7 times the previous technology making chip faster by 17% every year. Scaling down of CMOS technologies to 22nm has significant challenges in design. By reducing the dimensions many challenges like gate leakage, short channel effect (SCE), low voltage operation & delay comes into picture. Thus paper presents the past work done in design of nanoscale MOSFETs. The multi gate MOSFETs structure is considered as important candidates for CMOS scaling to reduce short channel effect. Gate All Around (GAA) & Double Gate (DG) are another design used to reduce SCE & suitable for low voltage operation. Use of Silicon on Insulator (SOI) for the thin short channel, Lower parasitic capacitance, Resistance to Latchup & has 10-20% higher switching speed. This paper shows the various challenges in design of MOSFET & various methods or techniques for increasing the performance of MOSFET at lower node.
***Keywords* -** ITRS, Short Channel Effect (SCE), Multi gate MOSFET & Silicon on Insulator (SOI).

I. INTRODUCTION

Since the fabrication of MOSFET, the minimum channel length has been shrinking continuously. The motivation behind this decrease has been an increasing interest in high speed devices and in very large scale integrated circuits. Scaling the CMOS technology into nanometer regime require an innovative approach in overcoming a number of short channel effect (SCE). MOSFETs built on the sidewalls of silicon pillars are increasingly being studied as an alternative to standard planar MOSFETs for the scaling of CMOS into the nanometer regime. To increase the performance of device, both channel length and width must be reduced. Reducing the channel length shows the short channel effect in conventional bulk MOSFETs. When the MOSFET channel length is scaled down, the vertical dimensions, i.e. the gate oxide thickness and the source-drain junction depth must be scaled down as well, in order to keep the short-channel effects (SCE) within acceptable limits. Ideal scaling is, for several reasons, not always possible and SCE can be worse in the scaled-down technology. One of the main SCE is the reduction in the threshold voltage with decreasing channel length. Threshold voltage reduction causes the off-current of an MOS transistor to increase significantly, thus giving rise to higher static power dissipation. To comply with the requirements of technology scaling, devices have been designed with more complex doping profiles in an effort to maintain long channel behavior at short channel lengths.

The term "double gate" refers to a single gate electrode that is present on two opposite sides of the device. Similarly, the term "triple gate" is used for a single gate electrode that is folded over three sides of the transistor.Hence multi gate structure has been proposed to reduce the short channel effect. This structure not only reduces the SCE but also helps in threshold voltage roll-off and Drain-Induced Barrier Lowering (DIBL).

II. LITERATURE REVIEW

Interconnect Capacitance is one of the major parameter which decreases the performance of MOSFETs. Increase in Interconnect capacitance increases the power delay product which generally observed in Bulk MOSFETs. With the use of Dual Gate structure i.e FinFET, the device & interconnect capacitance improves. FinFET devices allow increase of electrical width without increasing device layout area and thus, interconnect capacitance is comparatively lower [1]. Thus helps in minimizing power delay product.

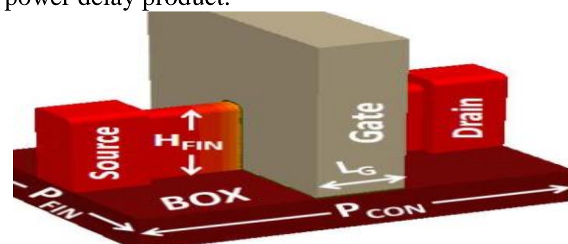
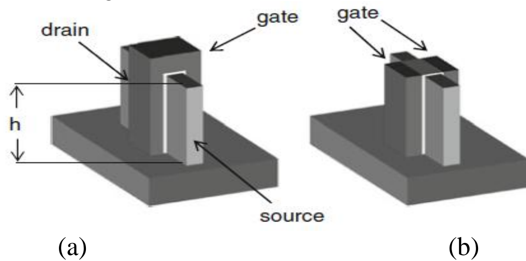


Fig 1. 3D model of the FinFET showing fin height (HFIN) perpendicular to the wafer surface.

$$\tau = \frac{C_{LOAD}V_{DD}}{I_{DRIVE}} \frac{(C_{GATE}+C_{INT})V_{DD}}{I_{DRIVE}}$$

$$P_{dyn} = \alpha C_{LOAD} V_{DD}^2 f = \alpha (C_{GATE} + C_{INT}) V_{DD}^2 f$$

where, CINT represents Interconnect Capacitance
Second problem which faces during scaling down technology is leakage current. Leakage current (sub-threshold + gate leakage) & device variability helps to increase yield. The suitable method to reduce the challenges occurred due to scaling, is FinFET structure with three different modes. SG-mode, in which FinFET gates are tied together; Low-power (LP)-mode, in which the back-gate bias is tied to a reverse-bias voltage to reduce sub-threshold leakage; and IG-mode, in which independent signals drive the two device gates [2].



(a) (b)
Fig 2. (a) SG-mode FinFET (b) IG-mode FinFET

The scaling limits of DG MOSFET & Triple Gate MOSFET using 2D & 3D computer simulation is also one of the problem which affect device performance. The fin height, fin thickness & fin width are considered to be an important factor for reducing SCE, Drain Induced Barrier Lowering (DIBL) and Sub-threshold Swing (SS). The 2D simulations show the gate-length (L) and fin-thickness (Tfin) ratio plays a key role while deciding the performance of the device [3]. While 3D simulation shows that both fin-thickness (Tfin) and fin-height (Hfin) can control the SCEs. Thus it is clear from paper that to get maximum ON current per unit width the relative ratio of Hfin and Tfin should be maximum at a given Tfin and Leff [3].

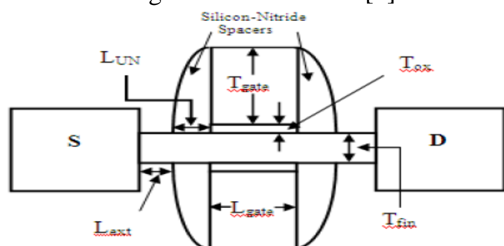


Fig 3. (DG) Double Gate FINFET structure

Double Gate structure is used to reduce short channel effect, OFF drive current and threshold voltage. Three different Double Gate Architectures is used & compared to increase device performance. All three architectures have some advantage and disadvantages. But out of these three architectures only Type III is preferred as it is more area efficient & less complicated than Type II [4]. Source /Drain series resistance & Mobility are found to be higher whereas saturation velocity is lower in FinFET [4]. Voltage gain is also higher in FinFETs as compared to bulk MOSFETs. The Fin width as important parameter to suppress the short channel effect & also helps in scaling down the gate length even further. The parasitic capacitance in FinFET is again important factor which is responsible for deceasing device performance.

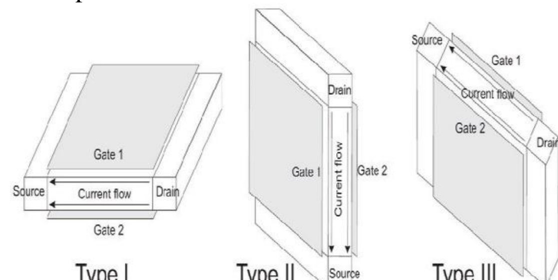


Fig 4. Double Gate Topologies: Type I (Planar), Type II (Vertical) & Type III (Vertical). The FinFET belongs to Type III category.

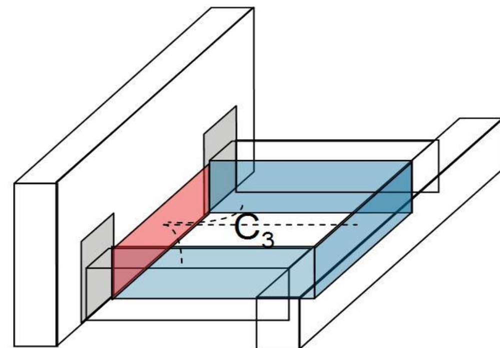


Fig 5. Important component of a FinFET's parasitic capacitance is the one existing between the gate and the inner walls of the source, drain and the access lines.

The dependence of parasitic capacitance on geometry is also considered to be a factor which affects during scaling down. The fringing capacitance Cfr and overlap capacitance Cov are the dominant parasitic capacitances in n fin DG FinFET[5].

$$C_{g,Total} = C_{in} + C_p$$

Where Cin – Intrinsic Capacitance & Cp – Parasitic Capacitance between gate & S/D

To reduce the overlap capacitance, use thick hard mask if gate oxide thickness is not flexible to adjust. The parasitic gate model is useful to calculate the delay. The minimum gate resistance dependent on geometry also derived from n Fin DG FinFETs [5]. Capacitive coupling with parasitic resistances even

dominates device characteristics. Through the comparison of multi fin FinFETs with the same device width, it reveals that the two-fin architecture provides not only the lowest equivalent gate resistance but also the smallest device delay [5].

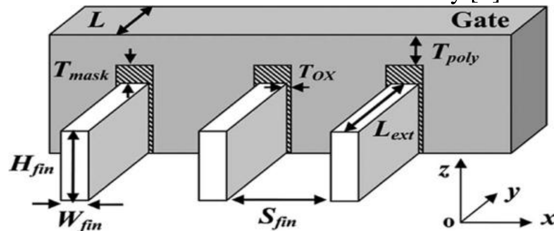


Fig 6. Three-dimensional structure of a three-fin (n = 3) DG FinFET. Wfin and Hfin denote the fin width and fin height, respectively. Tmask is the thickness of the hard mask above the fin. Tpoly is the geometrical thickness of the poly silicon gate on top of the hard mask. Lext represents S/D extension length. L is the channel length, and TOX is the thickness of gate oxide.

Off-state leakage current also plays a vital role in decreasing device performance during scaling down. The off- state leakage current also cause the power dissipation in MOSFETs. This off-state leakage current is reduced by using Dual-Gate structure of MOSFET. The Dual Gate structure provides additional gate length scaling by at least a factor of two [6]. The FinFET is used as it has Dual Gate structure.

The FinFET Structure is used to suppress the short channel effect which occurs due scaling down the node. The fin thickness (corresponding to twice the body thickness) is found to be critical for suppressing the short-channel effects [7]. The relation between the silicon Fin thickness and sub-threshold swing is used to increase the device performance. . The Fin thickness can also adjust to improve sub-threshold swing. FinFET used shows very high drive current and good short-channel behavior down to a gate length of 18 nm [7].

III. CONCLUSION

The scaling down to lower node MOSFETs has various challenges such as SCE, DIBL, High ON drive current, Sub- threshold voltage & parasitic capacitances. SCE can be reduced by properly adjusting Fin thickness twice the body thickness. Vertical Gate architectures can more area efficient & less complicated as compared to other. Use thick hard mask if gate oxide is not flexible to reduce parasitic capacitance. FinFET devices increase electrical width thus increasing device area which helps in reducing interconnect capacitance. It is clear from this paper that all these challenges are overcome by using various structures such as Double Gate (DG) MOSFETs, Multi-fin FinFETs & Gate All Around (GAA). Double gate & multi gate structure provide extra gate to reduce the problems caused due to scaling down of device. Thus proper design of these structures and the analyzing the each structure separately & the comparing the results with each other will yield the performance of MOSFETs.

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